19-2265; Rev 0; 12/01

MAX3670 Evaluation Kit

Evaluates: MAX3670

General Description

The MAX3670 evaluation kit (EV kit) is an assembled, surface-mount demonstration board that provides easy evaluation of the MAX3670 155MHz to 670MHz reference clock generator. The EV kit comes with external components and a 622.08MHz voltage-controlled crystal oscillator (VCXO).

Features

- **Fully Assembled and Tested**
- **5.0V Operation**

Component Suppliers

SUPPLIER	PHONE	FAX
AVX	843-448-9411	843-448-1943
Coilcraft	408-224-8566	408-224-6304
Murata	770-436-1300	770-436-3030
Vectron	1-88-VECTRON-1	1-888-PAX-VECTRON

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX3670EVKIT	-40°C to +85°C	32 QFN-EP*

**Exposed pad*

Electrical Component List

DESIGNATION	QTY	DESCRIPTION
C1, C4–C9, C12, C15, C16, C20, C22, C31–C35	17	0.1µF ±10% ceramic capacitors (0402)
C1A, C1B	2	0.015µF ±10% ceramic capacitors (0805)
C2, C3, C3A, C10, C11, C14, C19, C21, C23–C27, C29, C30	0	Open
C3B	1	6800pF ±10% ceramic capacitor (0805)
C13	1	1µF ±10% ceramic capacitor (0805)
C17	1	10µF ±10% tantalum capacitor
J1–J8, J11	9	SMA connectors (edge-mount)
J9, J10, J12, J15, J16	0	Open
J13, J14	2	Test points
JU1–JU5, JU7–JU10	9	1 × 3-pin headers
JU1–JU13	13	Shunts
JU6, JU11, JU12, JU13	4	1 × 2-pin headers
L1, L3, L4	0	Open
L2	1	56nH inductor

DESIGNATION	QTY	DESCRIPTION
R1, R11, R12, R13, R18–R21, R23, R24, R26, R27, R29, R31	0	Open
R1A, R1B	2	200kΩ ±1% resistors (0402)
R2	1	100Ω ±1% resistor (0402)
R3, R4, R6, R8, R10, R16, R17	7	332Ω ±1% resistors (0402)
R5, R7, R9, R14, R15, R22, R28, R30, R32	9	0Ω resistors (0402)
U1	1	MAX3670EGJ 32 QFN-EP
Y1	1	622.08MHz voltage-controlled SAW oscillator Vectron VS500A622
None	1	MAX3670 EV kit circuit board
None	1	MAX3670 EV kit data sheet
None	1	MAX3670 data sheet

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX3670 Evaluation Kit

Quick Start

1) Install shunts JU1, JU4, JU5, JU7, and JU10 between pins 1 and 2.
2) Install shunts JU11, JU12, and JU13.
3) Open shunts JU3 and JU6.
4) Install shunts JU2, JU8, and JU9 between pins 2 and 3.
5) Connect a 5V power supply to VCCA.
6) Connect ground to GND.
7) Apply a 1V_{P-P} differential clock input at 622.08MHz to REFCLK+ and REFCLK-.
8) Monitor MOUT+ and MOUT- with a 50Ω system. A 622.08MHz clock signal appears on the oscilloscope.

Adjustment and Control Descriptions*

COMPONENT	NAME	FUNCTION
JU1	GSEL1	Sets the phase-detector gain (K_{PD}) and the frequency divider ratio (N_2). Shunting between pins 1 and 2 sets to GND. Shunting between pins 2 and 3 sets to V_{CC} (see Table 1).
JU2	GSEL2	Sets the phase-detector gain (K_{PD}) and the frequency divider ratio (N_2). Shunting between pins 1 and 2 sets to GND. Shunting between pins 2 and 3 sets to V_{CC} (see Table 1).
JU3	GSEL3	Sets the phase-detector gain (K_{PD}) and the frequency divider ratio (N_2). Shunting between pins 1 and 2 sets to GND. Shunting between pins 2 and 3 sets to V_{CC} (see Table 1).
JU4	RSEL	Sets the predivider ratio for the reference input clock. Shunting between pins 1 and 2 sets to GND. Shunting between pins 2 and 3 sets to V_{CC} (see Table 2).
JU5	VSEL	Sets the predivider ratio for the VCO input clock. Shunting between pins 1 and 2 sets to GND. Shunting between pins 2 and 3 sets to V_{CC} (see Table 3).
JU6	—	Open when VCO is activated. Closed when VCO is disabled.
JU7	COMP	Sets the internal compensation of the op amp. Shunting between pins 1 and 2 sets the compensation to GND. Shunting between pins 2 and 3 sets the compensation to V_{CC}.
JU8	PSEL2	Sets the output clock divider. Shunting between pins 1 and 2 sets to GND. Shunting between pins 2 and 3 sets to V_{CC} (see Table 4).
JU9	PSEL1	Sets the output clock divider. Shunting between pins 1 and 2 sets to GND. Shunting between pins 2 and 3 sets to V_{CC} (see Table 4).
JU10	POLAR	Sets the polarity of the op amp. Shunting between pins 1 and 2 sets the polarity to GND. Shunting between pins 2 and 3 sets the polarity to V_{CC}.

**See Quick Start first.*

Adjustment and Control Descriptions (continued)

COMPONENT	NAME	FUNCTION
JU11	—	Ensure that shunt is installed.
JU12	—	Ensure that shunt is installed.
JU13	—	Ensure that shunt is installed.

Table 1. Gain Logic Pin Setup

INPUT PIN GSEL1	INPUT PIN GSEL2	INPUT PIN GSEL3	K_{PD} (µA/UI)	DIVIDER RATIO N
V_{CC}	V_{CC}	V_{CC}	20	1
OPEN	V_{CC}	V_{CC}	20	2
GND	V_{CC}	V_{CC}	20	4
V_{CC}	OPEN	V_{CC}	20	8
OPEN	OPEN	V_{CC}	20	16
GND	OPEN	V_{CC}	20	32
V_{CC}	GND	V_{CC}	20	64
OPEN	GND	V_{CC}	20	128
GND	GND	V_{CC}	20	256
V_{CC}	V_{CC}	GND	20	512
OPEN	V_{CC}	GND	20	1024
V_{CC}	V_{CC}	OPEN	5	1
OPEN	V_{CC}	OPEN	5	2
GND	V_{CC}	OPEN	5	4
V_{CC}	OPEN	OPEN	5	8
OPEN	OPEN	OPEN	5	16
GND	OPEN	OPEN	5	32
V_{CC}	GND	OPEN	5	64
OPEN	GND	OPEN	5	128
GND	GND	OPEN	5	256
V_{CC}	OPEN	GND	5	512
OPEN	OPEN	GND	5	1024

Table 2. Reference Clock Divider

INPUT PIN RSEL	REFERENCE CLOCK INPUT FREQ (MHz)	DIVIDER RATIO (N_3)	PREDIVIDER OUTPUT FREQ (MHz)
V_{CC}	77.76	1	77.76
OPEN	155.52	2	77.76
GND	622.08	8	77.76

Table 3. VCO Clock Divider

INPUT PIN VSEL	VCO CLOCK INPUT FREQ (MHz)	DIVIDER RATIO (N_1)	PREDIVIDER OUTPUT FREQ (MHz)
V_{CC}	77.76	1	77.76
OPEN	155.52	2	77.76
GND	622.08	8	77.76

Table 4. Optional Clock Output Divider

INPUT PIN PSEL1	INPUT PIN PSEL2	VCO TO POUT DIVIDE RATIO
V_{CC}	V_{CC}	1
GND	V_{CC}	2
V_{CC}	GND	4
GND	GND	8

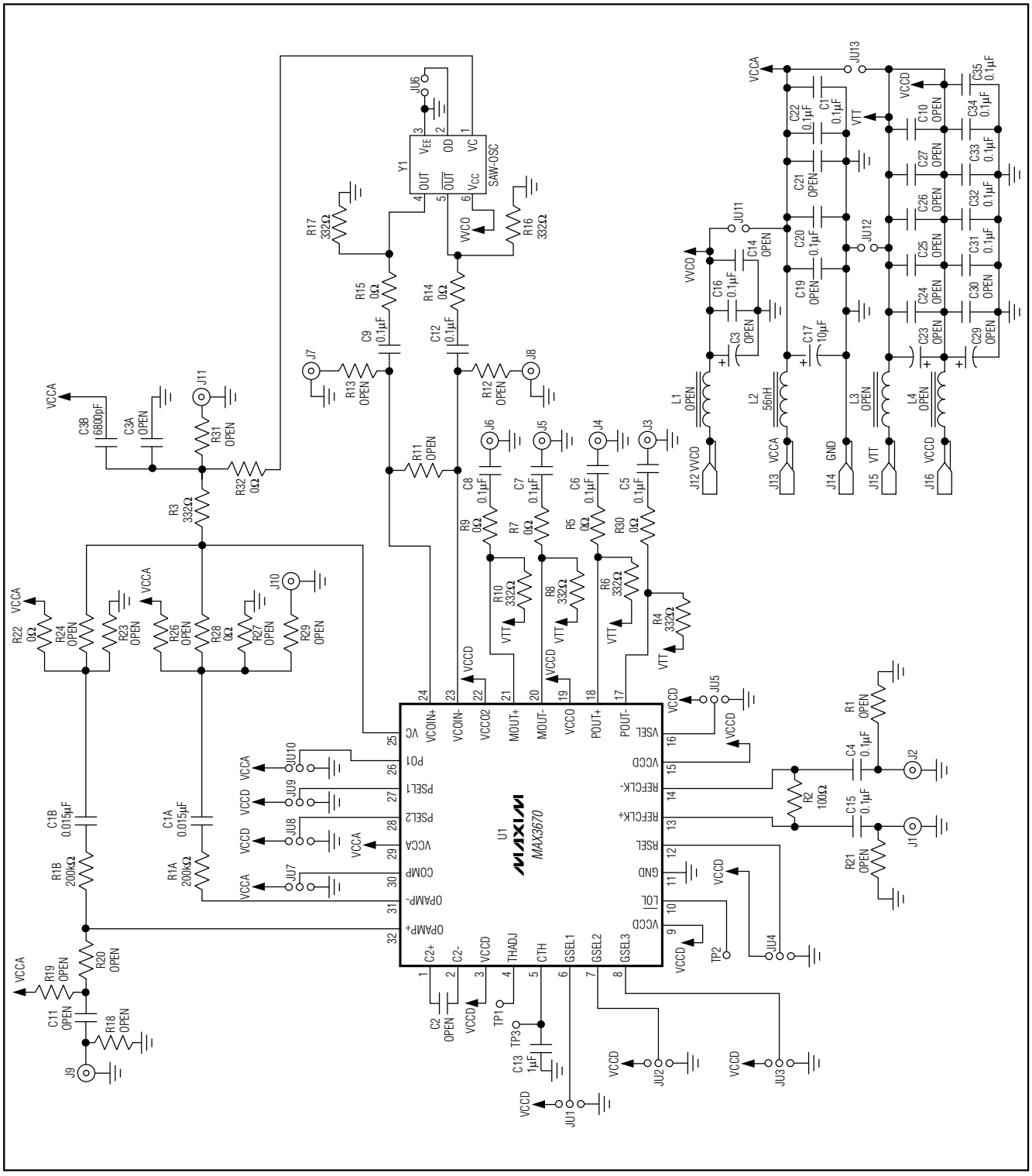

Figure 1. MAX3670 EV Kit Schematic

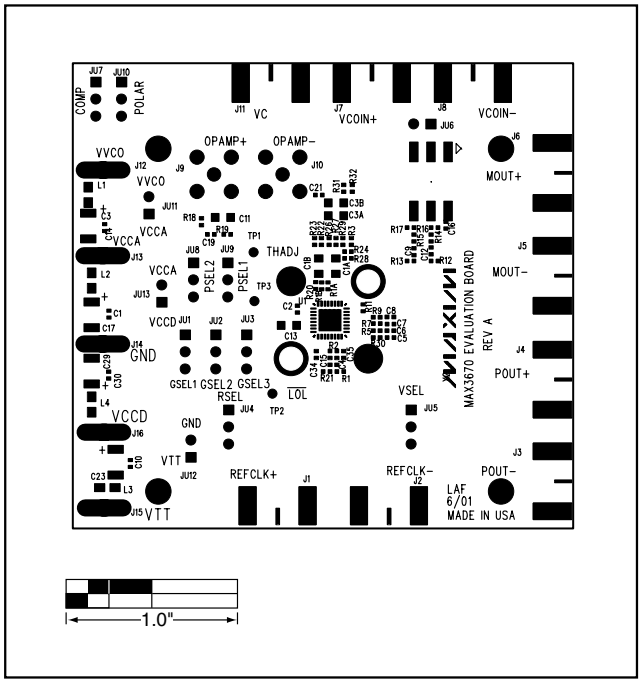

Figure 2. MAX3670 EV Kit Component Placement Guide—Component Side

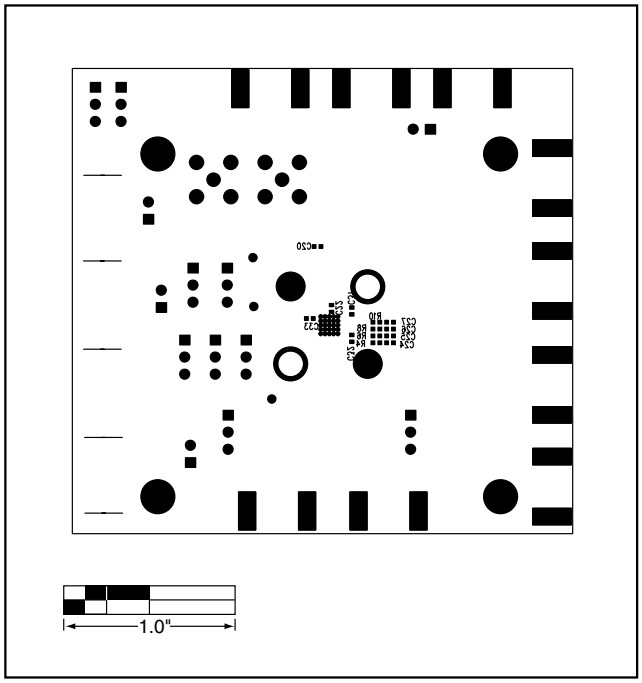

Figure 3. MAX3670 EV Kit Component Placement Guide—Solder Side

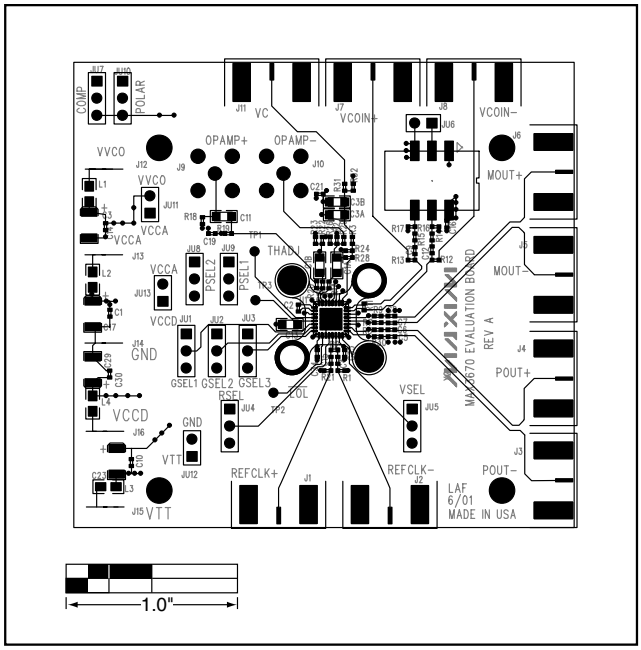

Figure 4. MAX3670 EV Kit PC Board Layout—Component Side

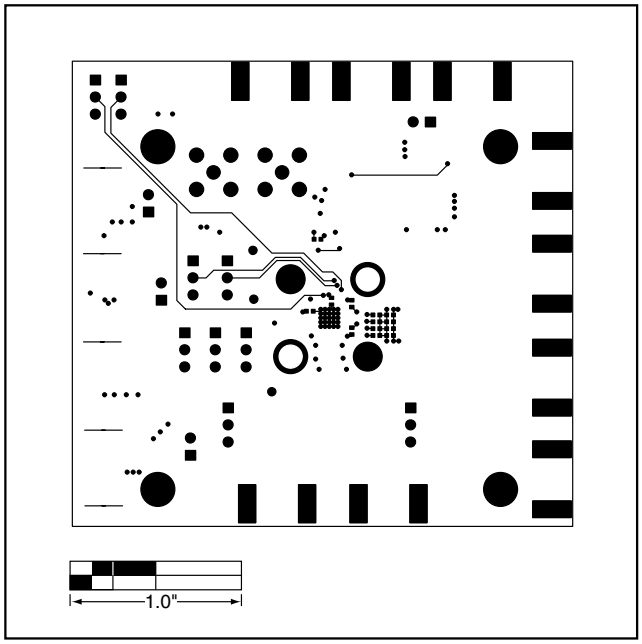

Figure 5. MAX3670 EV Kit PC Board Layout—Solder Side

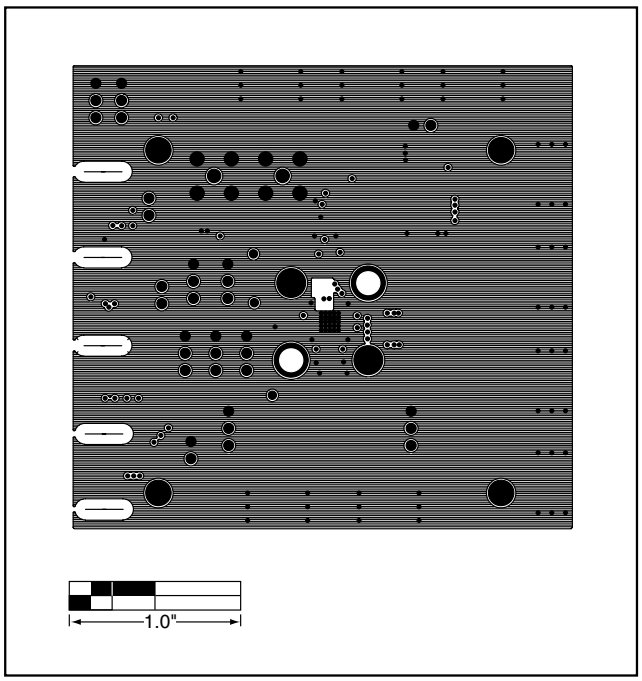

Figure 6. MAX3670 EV Kit PC Board Layout—Ground Plane

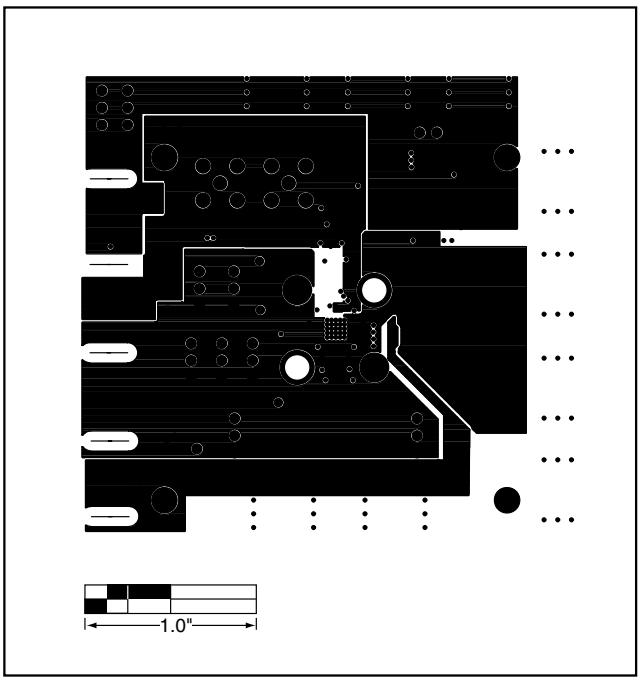

Figure 7. MAX3670 EV Kit PC Board Layout—Power Plane

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